Detailed Action

1. This Office Action is submitted in response to the amendment filed 7-28-2008, wherein claims 1, 8, 15, 16, 21, 22, and 25 have been amended, claims 13, 14, and 20 have been cancelled, and claims 32 and 33 have been added. Claims 1, 4-9, 12, 15-19, 21-25, and 28-33 are pending.

Response to Arguments

2. Applicant's arguments filed 7-28-2008 have been fully considered but they are not persuasive.

3. Applicant argues at pages 8 of the remarks that, Koezuka and Jeon, either alone, or in combination, fail to teach or suggest the limitations recited by amended independent claim 1 including wherein the voltage source is configured to attract ions to implant in a buffer layer of the sample, the buffer layer proximate the high-k dielectric layer.

4. The examiner disagrees for the following reasons;

(a) Koezuka discloses controlling accuracy of implantation depth or dopant depth by varying the acceleration voltage and the dopant material at Col. 1, line 12-29; and Col. 10, line 4-15,

(b) Koezuka discloses implanting in a plurality of layers at Col. 6, line 32-38,

(c) Jeon discloses disclosing implanting ions in high-k dielectric layers at Col. 4, line 1-10; and Col. 14, line 9-20,

(d) Yamada discloses the use of a 15 keV acceleration voltage to implant BF^2 in a 1000A° buffer layer located between a 200A° SiO_2 layer and an SOI layer of silicon at [0130]. See also Figure 3A below.

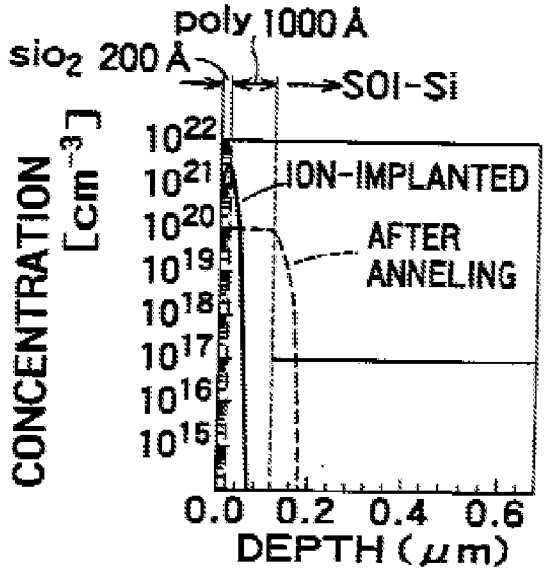

FIG. 3A

One of ordinary skill would interpret from the above that Koezuka and Jeon disclose fabrication of a device with ion implantation having plural layers that includes the structure of a high-k dielectric layer adjacent a buffer layer, and implanting a desired dopant concentration at a desired depth in a layer by varying the acceleration voltage, and since Yamada discloses implanting ions into a buffer layer located adjacent a dielectric layer, one of ordinary skill would recognize that implanting ions into a buffer layer adjacent a high-k dielectric layer is an obvious choice of known prior art implantation parameters.

Therefore the examiner has determined that the amended claim 1 limitation of using a voltage source to attract ions to implant them in a buffer layer proximate a high-

k dielectric layer is disclosed in the combination of Koezuka, Jeon, and Yamada, as described in the rejection below.

5. The rejection of claims 1, 4-9, 12, 15-19, 21-25, and 28-33 under 35 USC 103(a) are maintained.

6. All claims stand finally rejected.

Claims Rejection – 35 U.S.C. 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 32, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,995,079 to Koezuka, in view of Jeon, U.S. Patent No. 6,790,755, and in further view of Yamada, US Pat Pub No 2001/0054746.

4. Regarding claim 1, Koezuka teaches an ion implantation apparatus at Col. 3, line 21-40, as shown below in Figure 2 having the following claimed elements;

(a) Vacuum chamber 102,

(b) Vacuum pumping system 106,

(c) Gas supplied from tanks 110-112.,

(d) Plasma ion source 101,

(e) Dopant ions produced from Group 2, 3, 5, and 6 elements; e.g. B, Al, Ga, In, and Zn, are supplied from tanks 110 and 111,

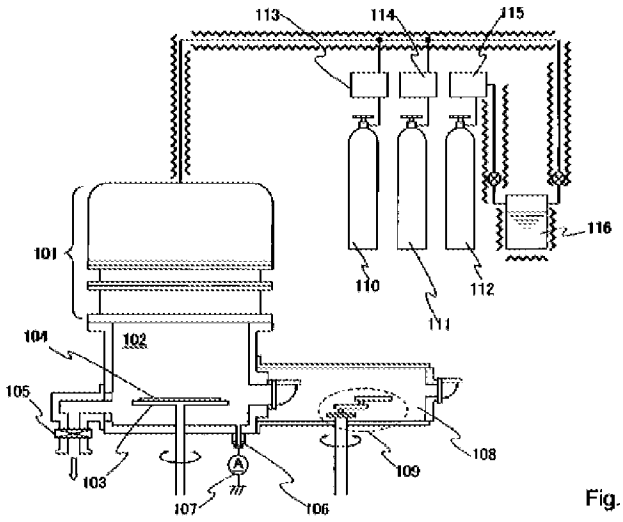

Fig. 2

(f) Plural power supplies (voltage sources) to ionize the gas and accelerate the resultant ions, via a bias applied to the substrate 104. See also Col. 7, line 11-16.

(g) Wafer support stage 103,

Koezuka also discloses fabrication of semiconductor devices by ion implantation of a stack of layered films including conductive metal layers, and insulating films such as silicon oxide and silicon nitride, that are doped by ion implantation, as well as providing controlled diffusion of alkali and alkaline earth metals into the doped films. Col. 5, line 15-38; and Col. 6, line 38-55.

Koezuka further discloses controlling accuracy of implantation depth or dopant depth by varying the acceleration voltage and the dopant material at Col. 1, line 12-29; and Col. 10, line 4-15.

5. Koezuka fails to disclose implanting ions into a high-k dielectric layer having a k value greater than 9.

6. Jeon teaches ion implantation after deposition of alternating sub-layers of high-k dielectric and are high-k dielectric materials on a semiconductor substrate. The high-K dielectric materials have a K value of about 20 or more. Such high-K dielectric materials include, for example, HfO_2, ZrO_2, and Ta2 O_5. Col. 4, line 1-10; and Col. 14, line 9-20.

Jeon also discloses that silicon oxide has a dielectric constant K of approximately 3.9, and silicon nitride has a K of about 6 to 9. Col. 2, line 13-24.

Jeon modifies Koezuka to provide a semiconductor device with a composite dielectric layer formed by nitridation of plural high-k dielectric layers.

Therefore it would have been obvious to one of ordinary skill in the art that the apparatus and device fabrication technique of Koezuka can be modified to use ion implantation of high-k layers in accordance with Jeon, to provide a semiconductor device having a composite dielectric layer, thereby allowing the use of very thin dielectric layers to improve device performance.

7. The combination of Koezuka and Jeon fails to teach implanting ions into a buffer layer.

8. Yamada teaches a buffer layer 6 such as amorphous silicon or epitaxially grown single crystal silicon, silicides, or metals, or insulating films of BSG (boron silicate glass). See [0128] and [0141].

Yamada also discloses the use of a 15 keV acceleration voltage to implant BF^2 in the buffer layer located between a 200A° SiO_2 layer and an SOI layer of silicon at [0130]. See also Figure 3A below.

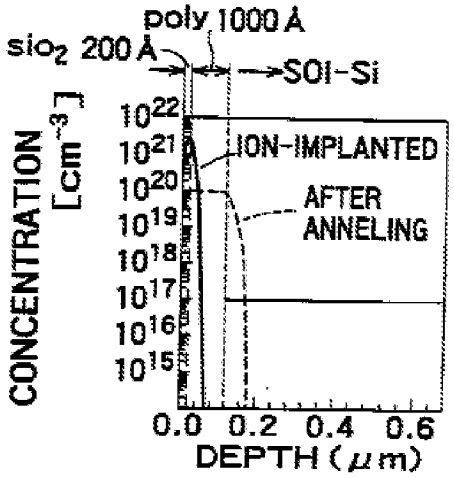

FIG. 3A

Yamada modifies Koezuka and Jeon to provide a structure made by stacking a buffer layer of 100 nm thick polysilicon on an SOI layer of silicon and implanting BF^2 ions through a 20nm thick silicon oxide film for later diffusion to a predetermined depth. See [0129]; and [0130].

Therefore it would have been obvious to one of ordinary skill to provide buffer layers on stacked dielectric layers that are implanted with ions where the doping concentration is later adjusted by diffusion to create a shallow base region in the depth direction, thereby producing a bipolar semiconductor device that exhibits excellent high-frequency property.

9. Regarding new claims 32 and 33 the combination of Koezuka and Jeon discloses the stack of layers as described above regarding claim 1.

10. Claims 4-9, 12, 15-19, 21-25, and 28-30, are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 6,995,079 to Koezuka, in view of Jeon, USPN 6,790,755, and in further view of USPN 6,518,195 to Collins.

11. Regarding claims 4-9, the combination of Koezuka and Jeon discloses the plasma ion implantation apparatus as described above regarding claim1, but fails to teach the use of a constant DC voltage supply for accelerating positive ions and repelling negative ions.

12. Collins discloses the use of AC supply 31 and DC supply 42 provides a constant positive or negative DC bias between the sample holder and the chamber wall (Col. 11, line 60-67), where a negative bias extracts positive ions toward (accelerate) the wafer.

One of ordinary skill in the implantation art recognizes that applying a negative bias to the sample would repel negative ions.

Therefore it would have been obvious to one of ordinary skill in the art that the ion implantation apparatus of Koezuka and Jeon, would use the AC and DC voltage sources of Collins to accelerate ions from the plasma to impinge on the wafer in order to control implantation of the ions.

13. Regarding claims 12, 15, and 16, the combination of Koezuka, Jeon, and Collins discloses the claimed high-K dielectric layers, buffer layers, and dopants as described above regarding claim1.

14. Regarding claim 17, Koezuka discloses forming a device having a plurality of insulating and conductive layers at Col. 6, line 32-48; and implanting ions into the plural layers at Col. 7, line 24-61, which would also include the use of adjacent high-k dielectric layers as described above regarding claim 1.

15. Regarding claims 18, and 19 the combination of Koezuka and Jeon teaches all the limitations therein as pointed out above regarding claim 1.

16. Regarding claims 20-22, the combination of Koezuka, Jeon, Collins and Yamada teaches the use of a buffer layer, as described above regarding claim 1.

17. Regarding claims 23 and 24, the combination of Koezuka, Jeon, Collins and Yamada teaches the voltage sources, as described above regarding claims 4-9.

18. Regarding claims 25, 28, and 29, the combination of Koezuka, Jeon, and Collins discloses the apparatus used in these method claims, as described above regarding claims 4-9.

19. Regarding claim 30, Koezuka discloses implant dose rates between 10^{13} and 10^{16} at Col. 7, line 27-34.

20. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 6,995,079 to Koezuka, in view of Jeon, USPN 6,790,755, in further view of USPN 6,518,195 to Collins, and in still further view of USPN 6,248,662 to Wu.

21. Regarding claim 31, the combination of Koezuka, Jeon, and Collins fails to teach implanting ions with an energy range of 5-10 kev.

22. Wu teaches the use of an ion implantation sources where BF3 ions are implanted at a typical energy of about 5.0 KeV. Col. 3, line 5-17.

23. Wu modifies Koezuka and Jeon to provide an ion source where the energy of the implanted ions is restricted so that the implanted ions are only concentrated in the surface of the first dielectric layer.

24. Therefore it would have been obvious to one of ordinary skill to implant ions at energies that have been selected to form void-free dielectric layers.

Conclusion

7. The Amendment filed on 7-28-2008 has been considered but is ineffective to overcome the references cited in the Office Action mailed 5-28-2008.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications should be directed to Phillip Johnston whose telephone number is (571) 272-2475. The examiner can normally be reached on Monday-Friday from 7:00 am to 4:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiners supervisor Robert Kim can be reached at (571) 272-2293. The fax phone number for the organization where the application or proceeding is assigned is 571 273 8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PJ
October 21, 2008

/ROBERT KIM/

Supervisory Patent Examiner, Art Unit 2881